

FIG. 1 (PRIOR ART)

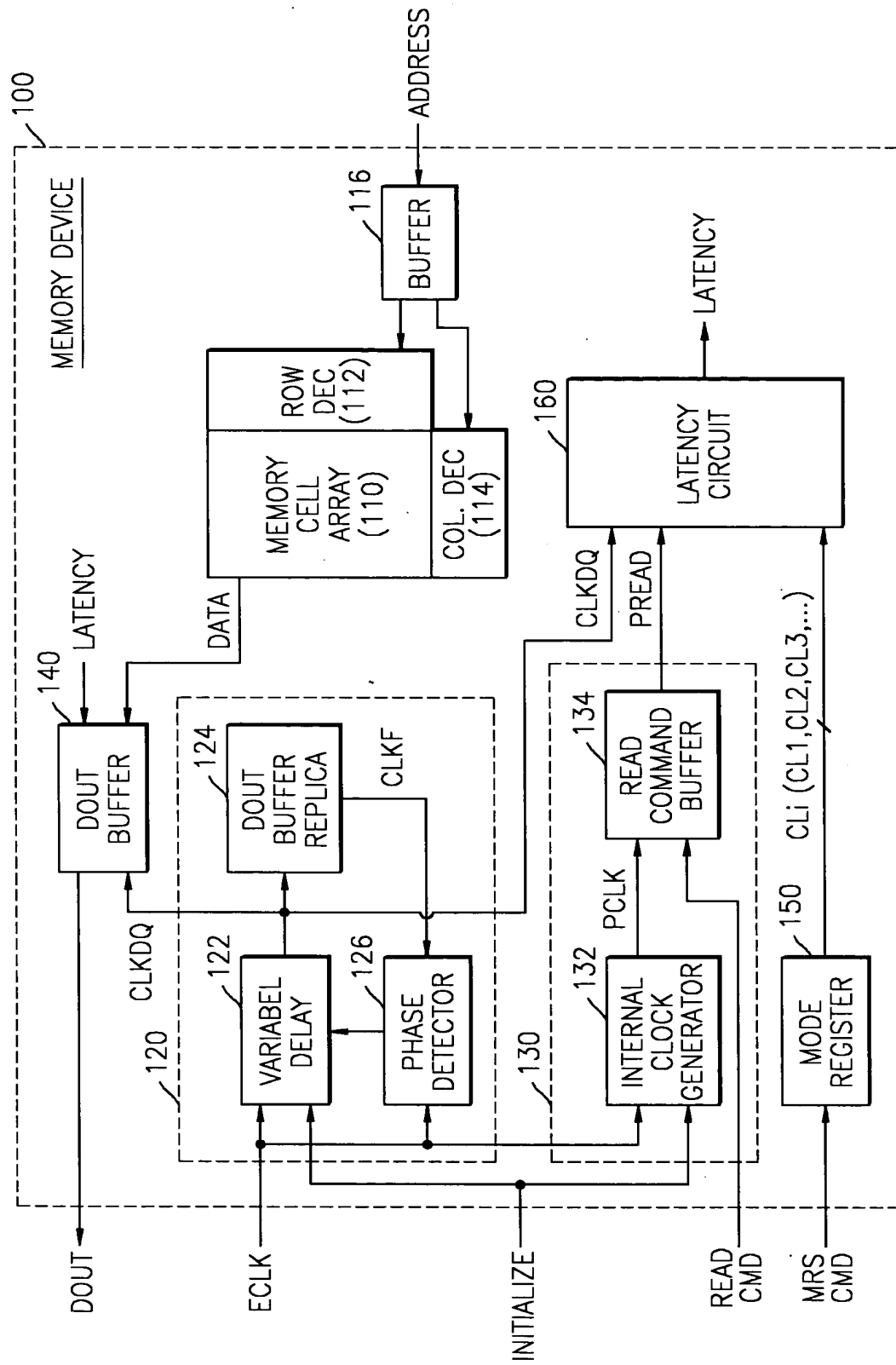


FIG. 2 (PRIOR ART)

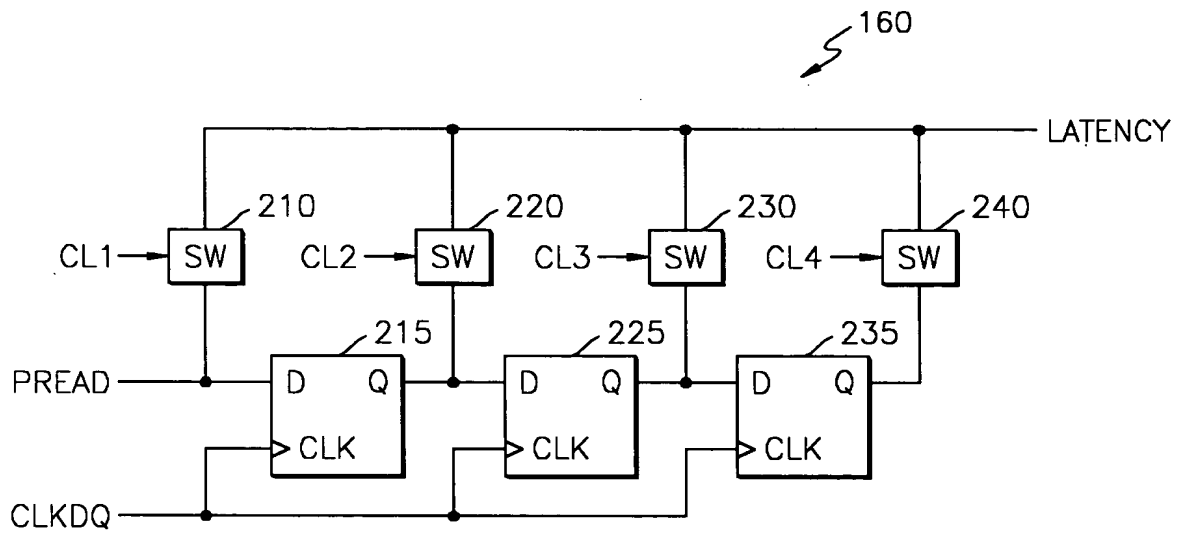


FIG. 3A (PRIOR ART)

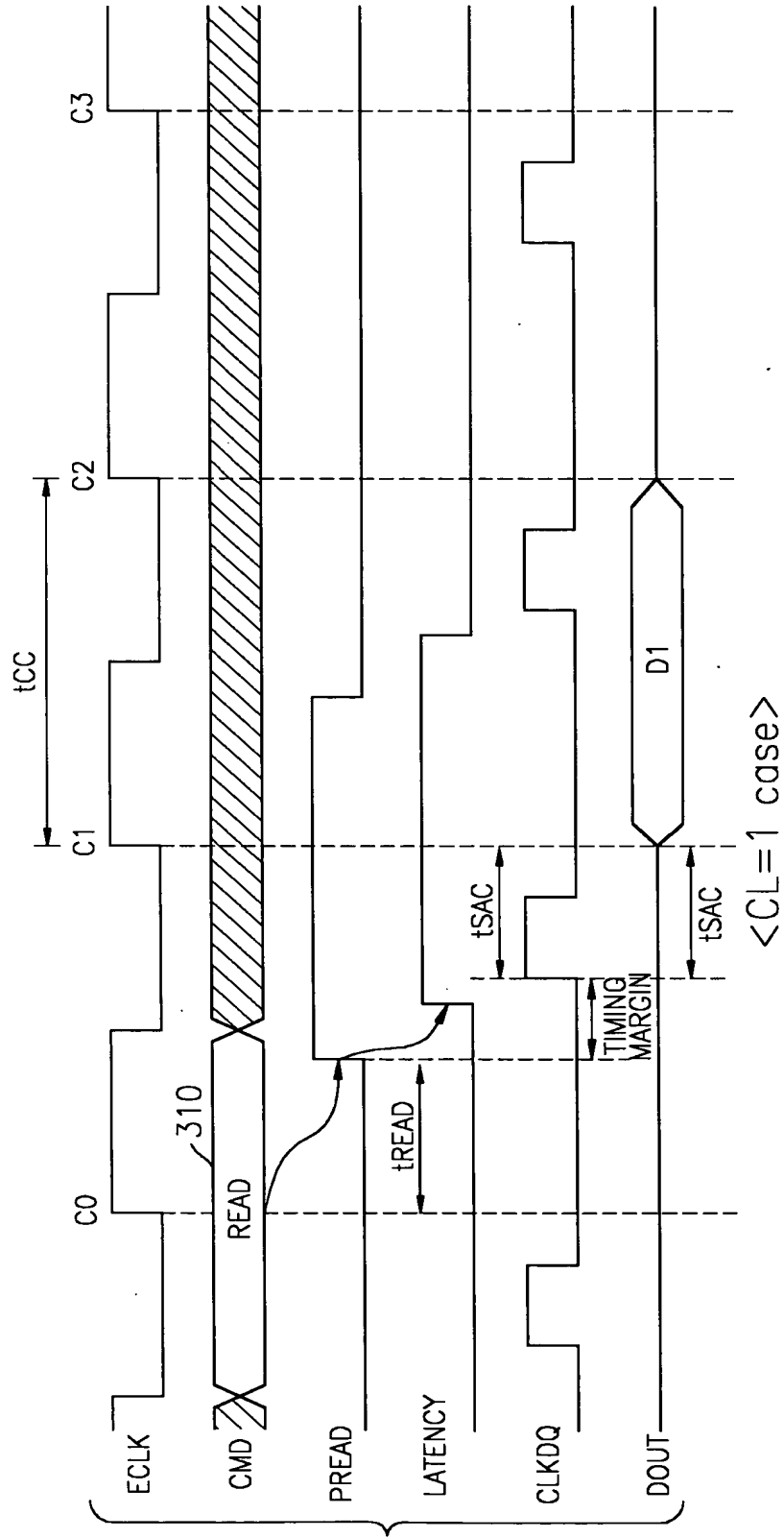


FIG. 3B (PRIOR ART)

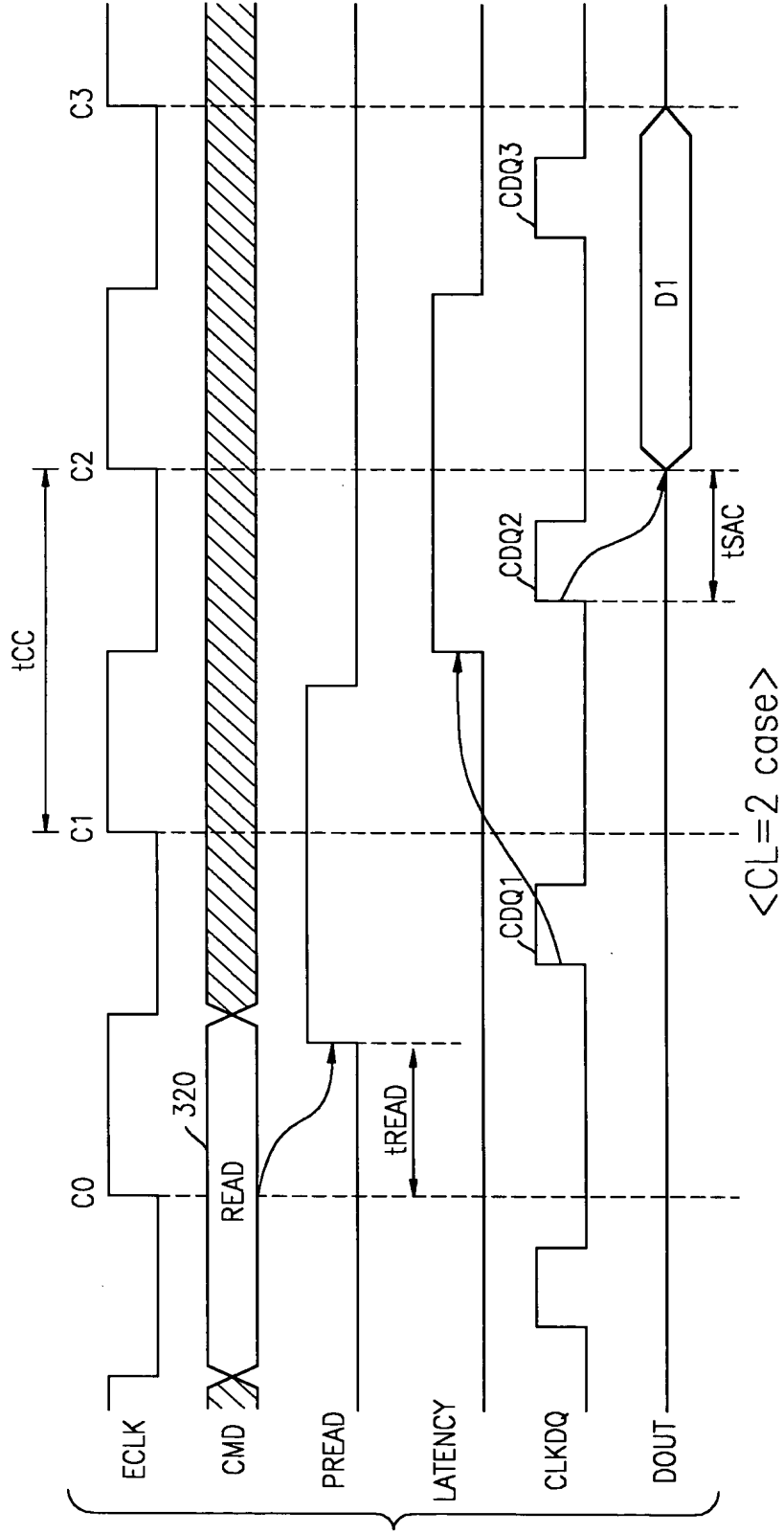


FIG. 3C (PRIOR ART)

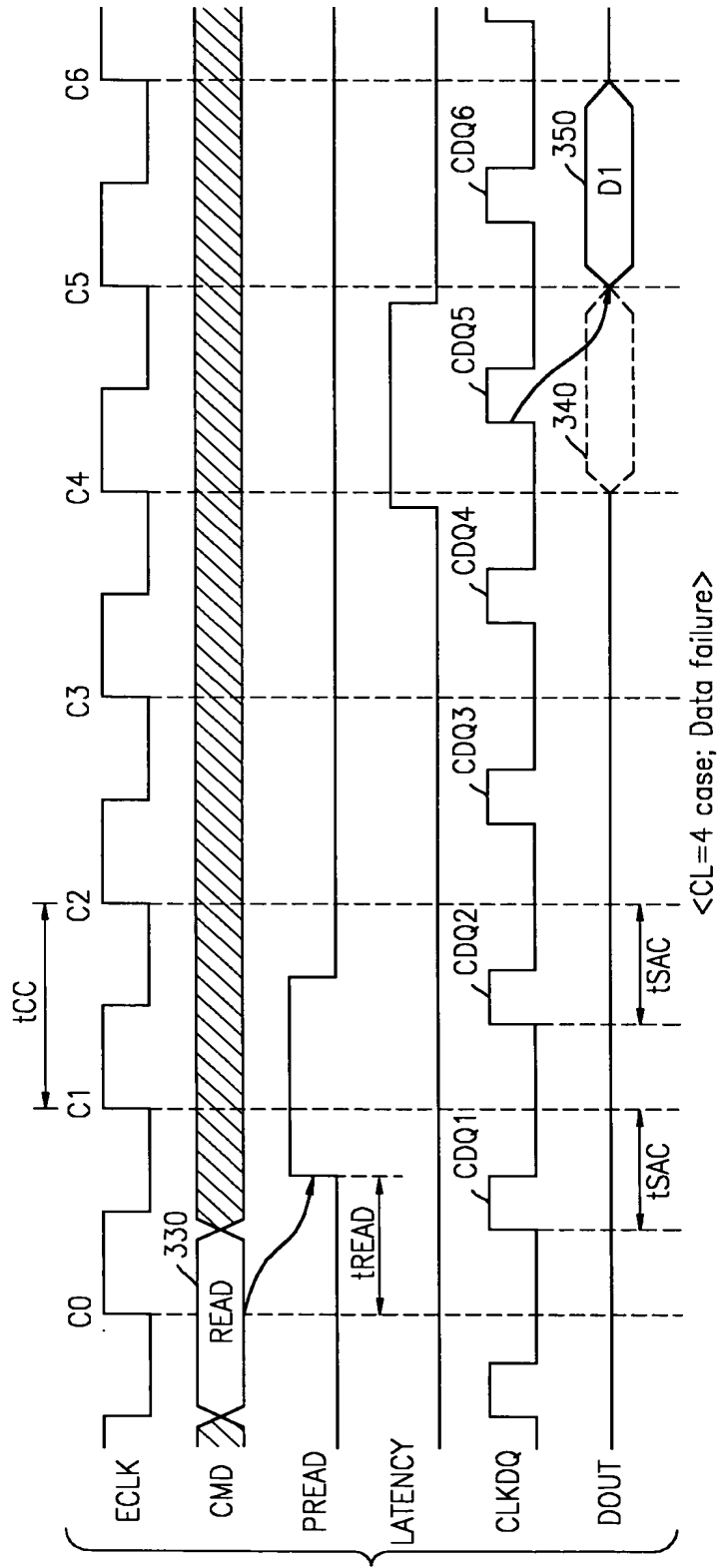


FIG. 4A

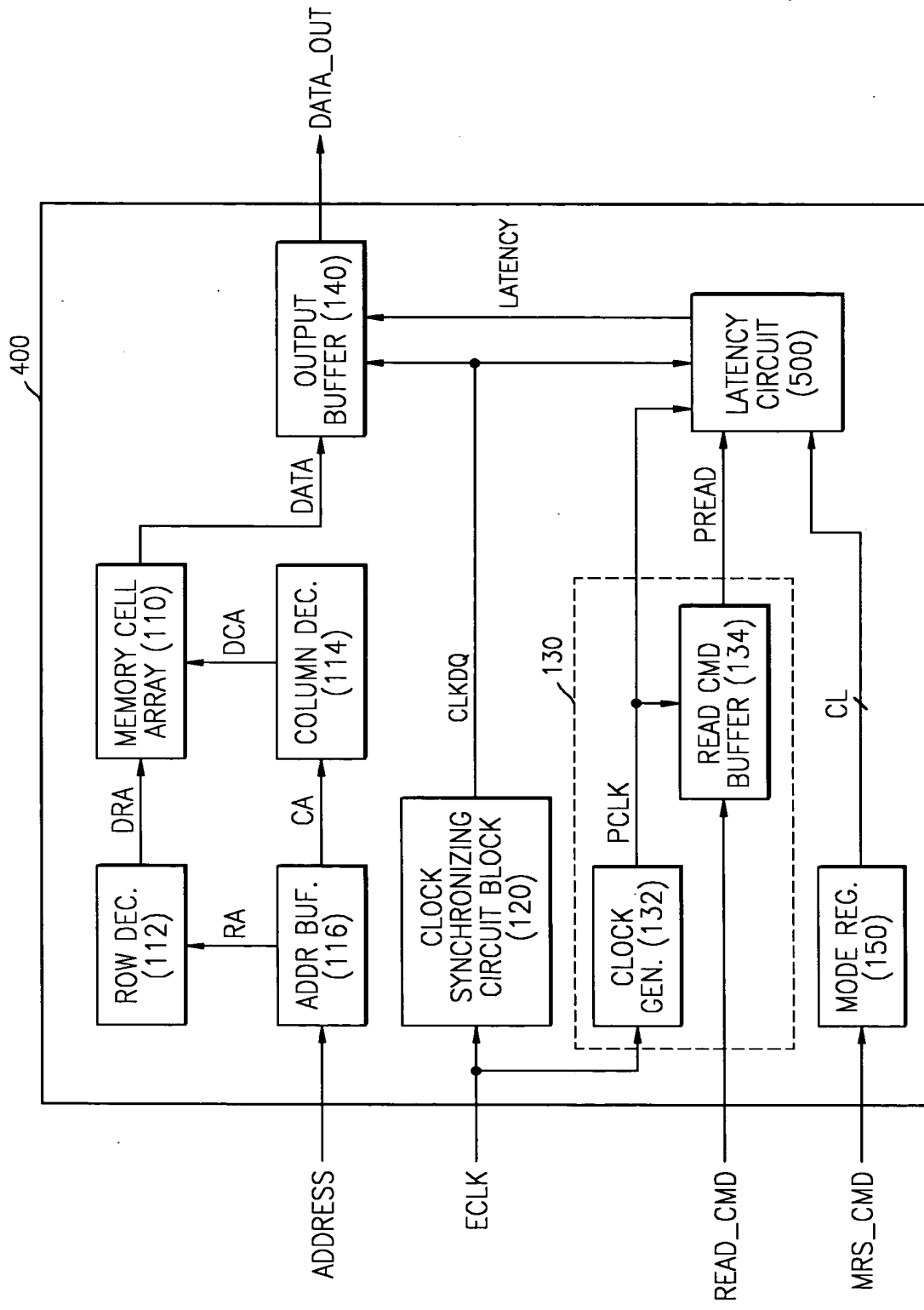


FIG. 4B

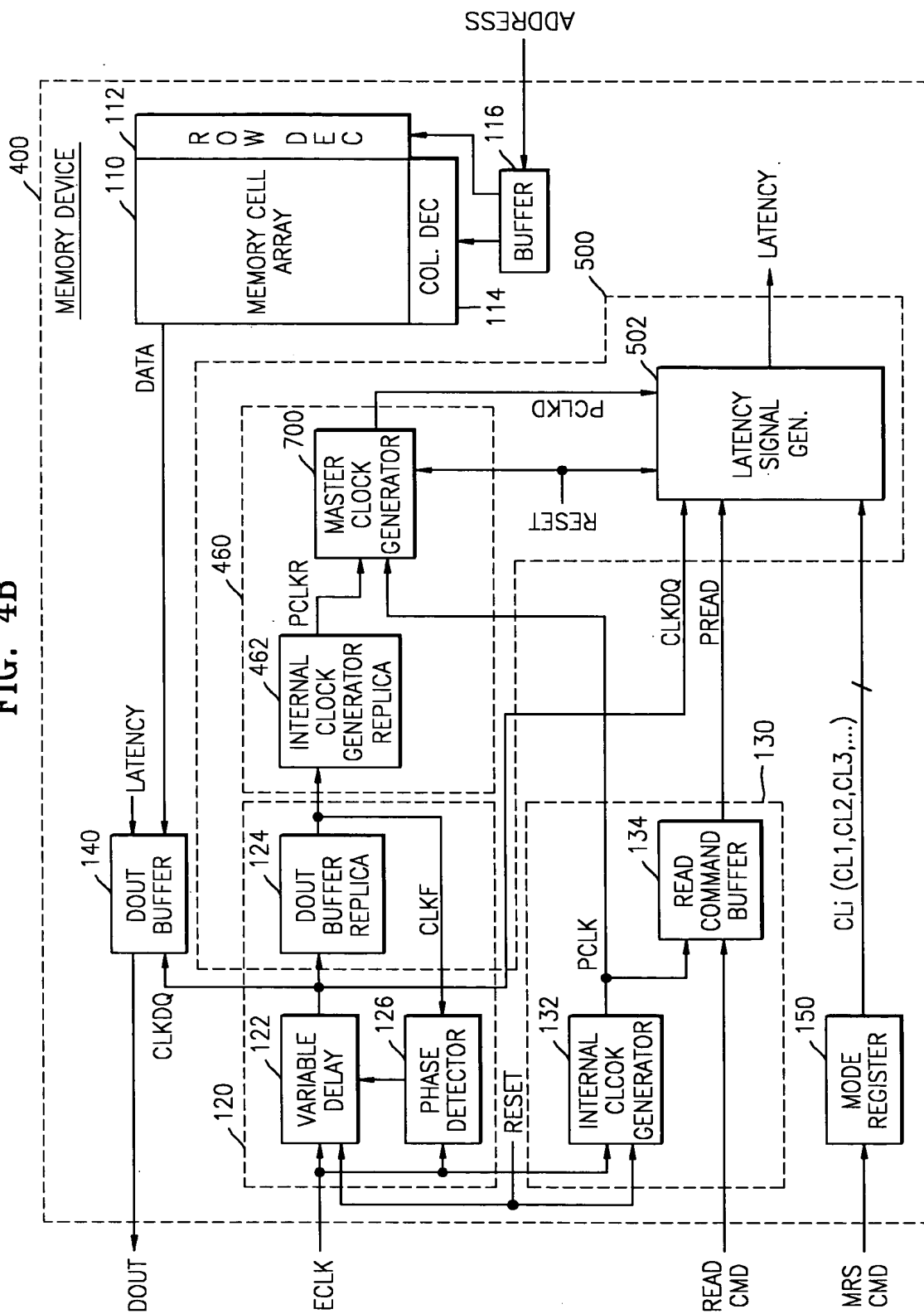


FIG. 4C

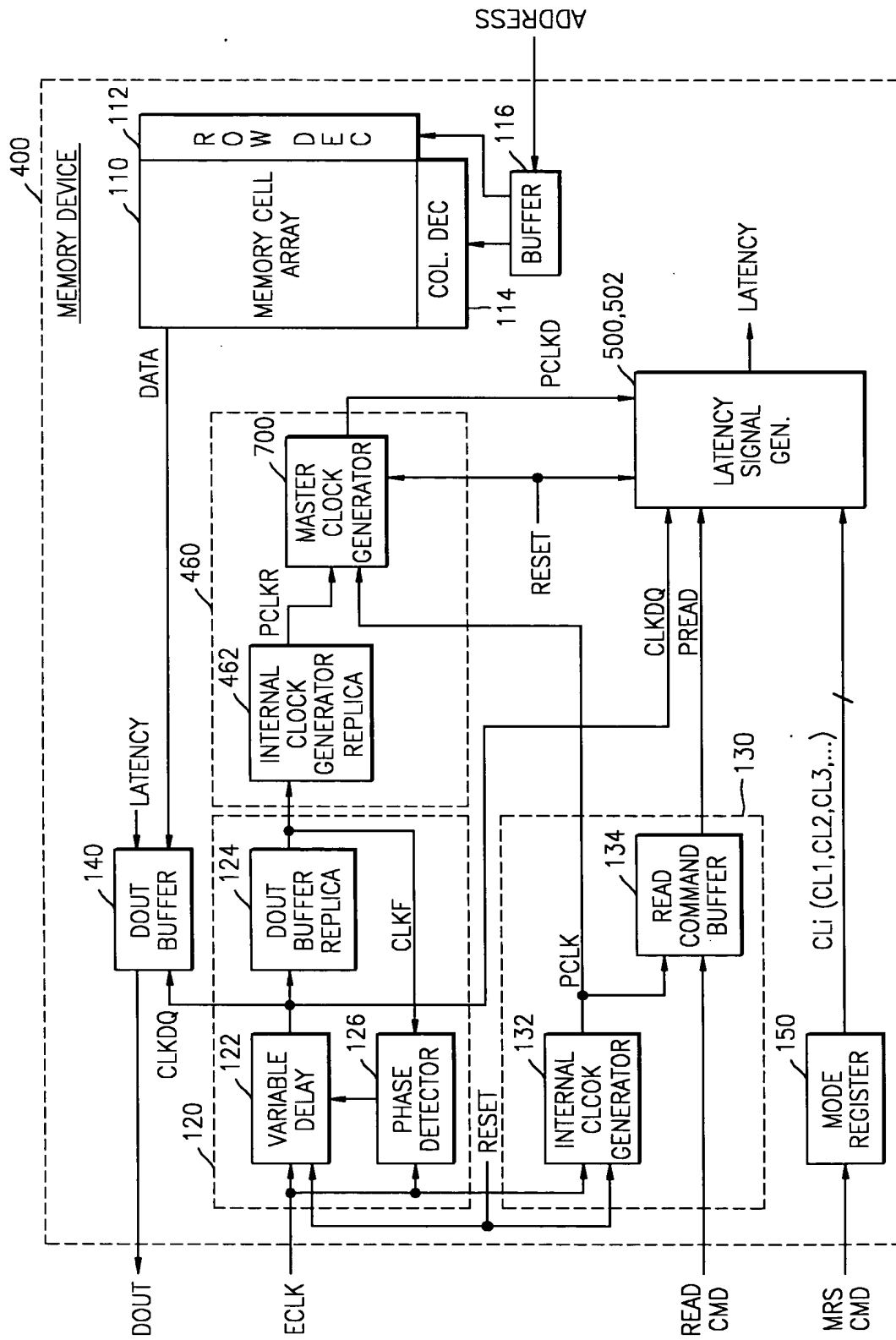


FIG. 5

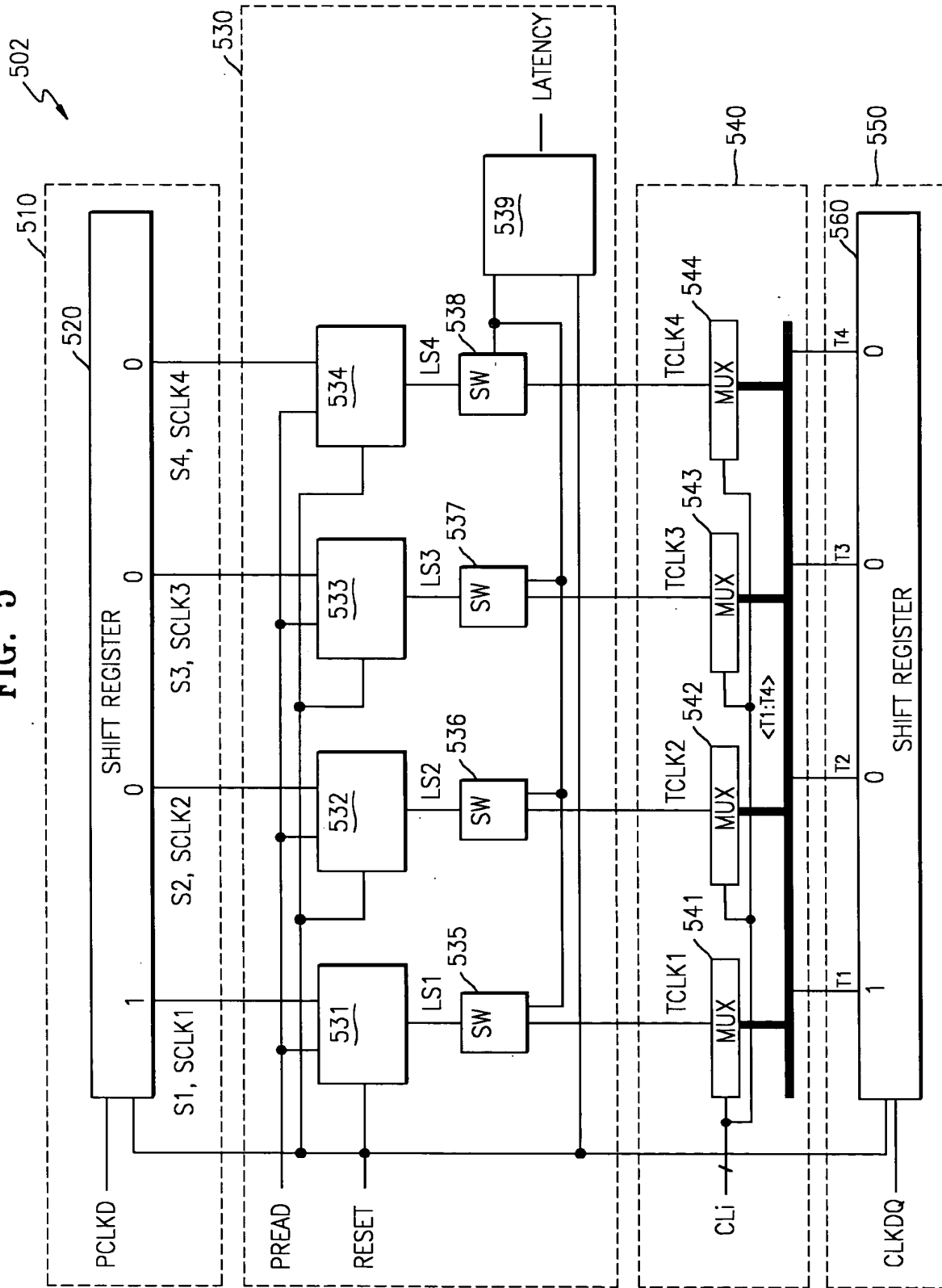


FIG. 6

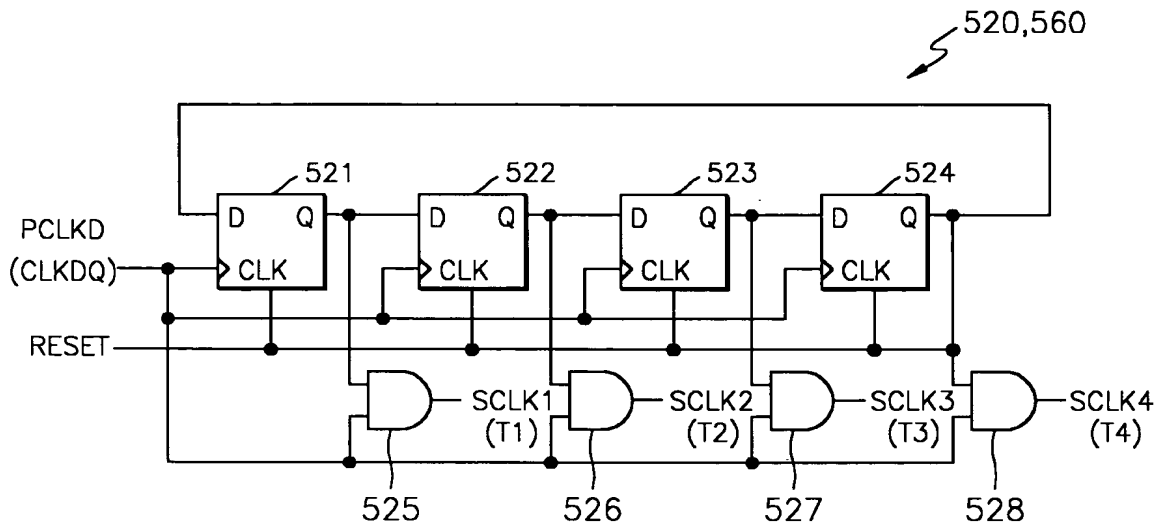


FIG. 7

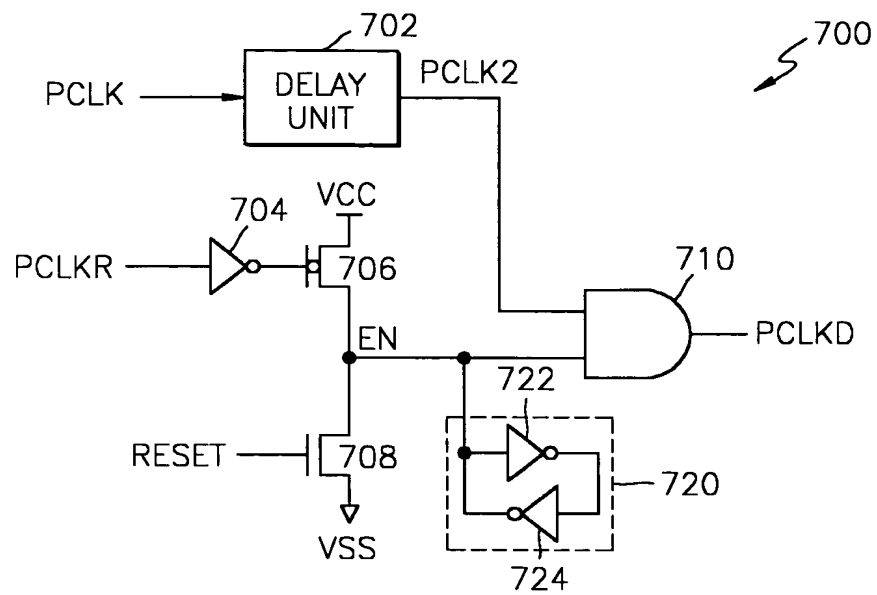
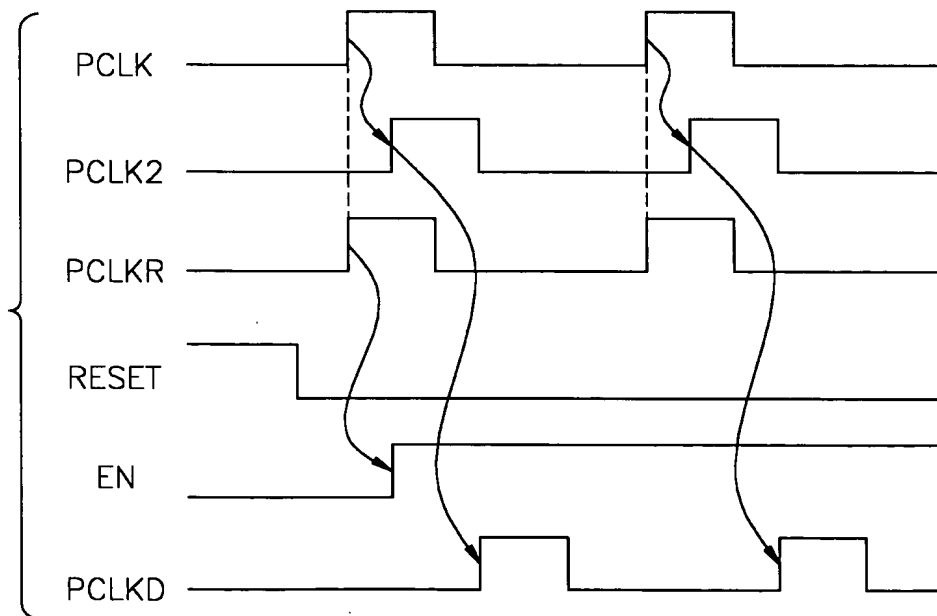


FIG. 8



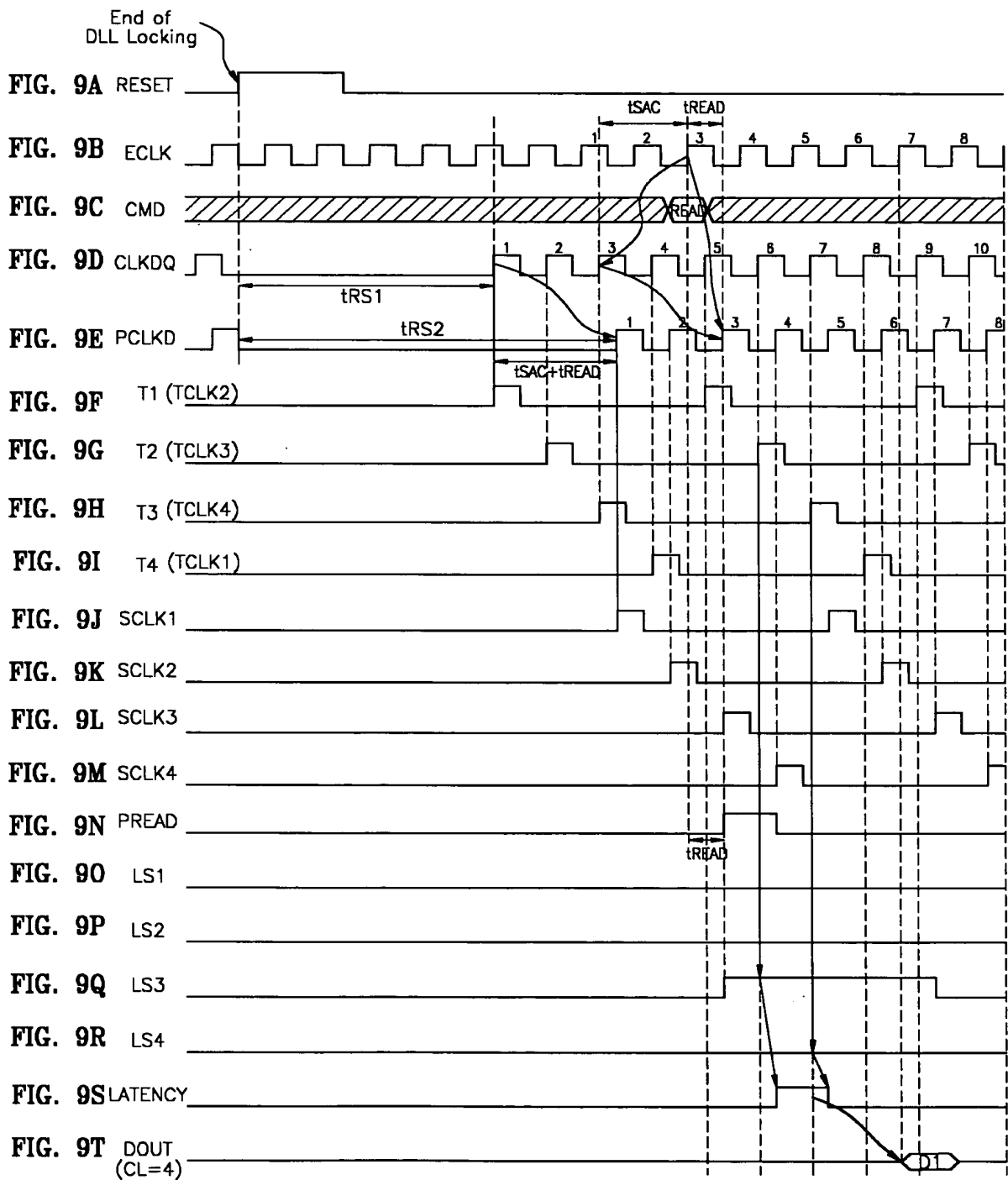


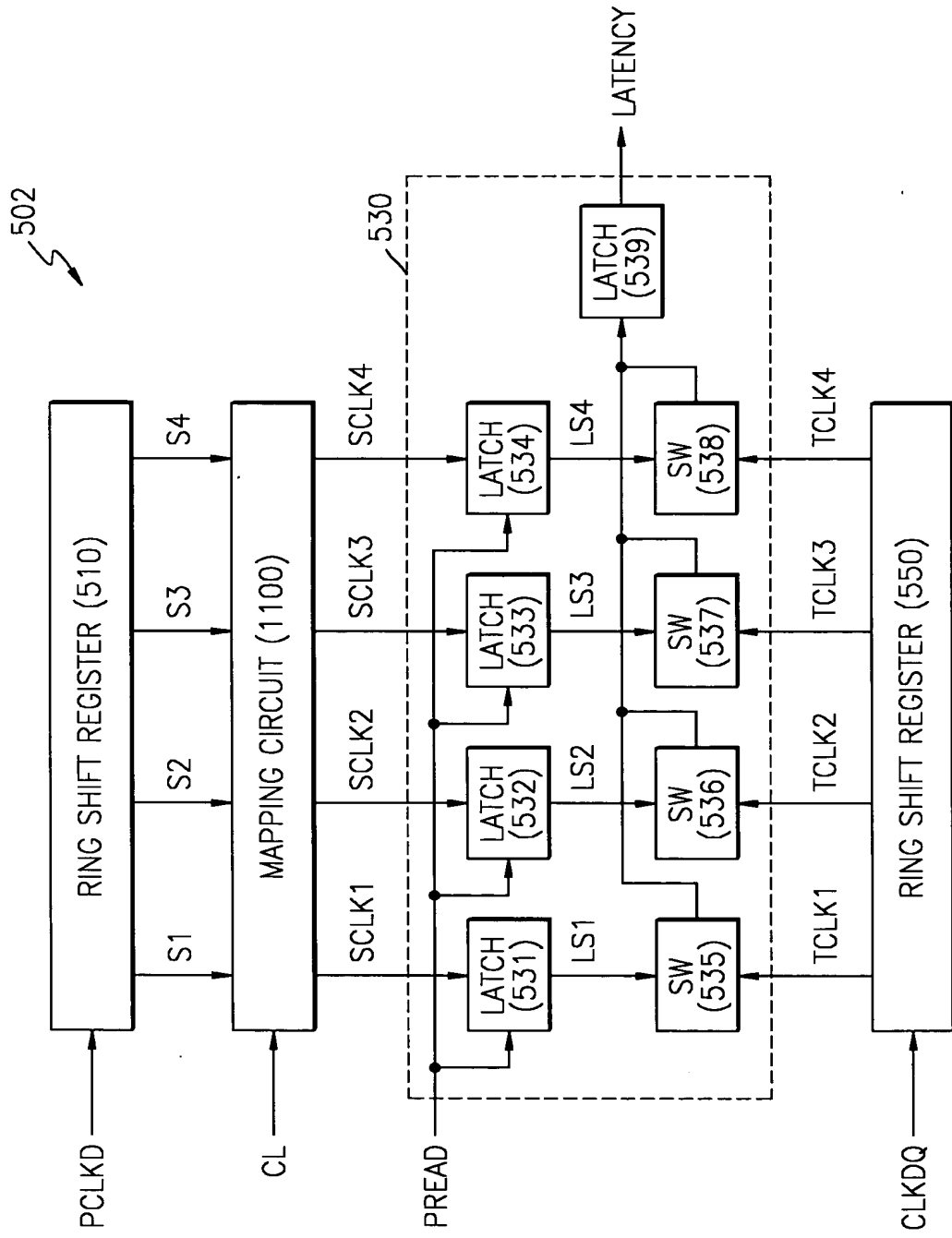
Figure 1 shows four circuit diagrams (541, 542, 543, 544) illustrating different clock signal distributions. Each diagram has four inputs (T1, T2, T3, T4) and one output (TCLK1, TCLK2, TCLK3, TCLK4). The inputs are connected to a common bus through inverters (CL1-CL5). The output is taken from the common bus.

- Diagram 541:** Inputs T1, T2, T3, T4 are connected to inverters CL1, CL2, CL3, CL4 respectively. The output TCLK1 is taken from the common bus.
- Diagram 542:** Inputs T1, T2, T3, T4 are connected to inverters CL4, CL5, CL2, CL3 respectively. The output TCLK2 is taken from the common bus.
- Diagram 543:** Inputs T1, T2, T3, T4 are connected to inverters CL3, CL4, CL5, CL2 respectively. The output TCLK3 is taken from the common bus.
- Diagram 544:** Inputs T1, T2, T3, T4 are connected to inverters CL2, CL3, CL4, CL5 respectively. The output TCLK4 is taken from the common bus.

FIG. 10B

CL MODE	TCLK1	TCLK2	TCLK3	TCLK4
4	T4	T1	T2	T3
5	T1	T2	T3	T4
2	T2	T3	T4	T1
3	T3	T4	T1	T2

FIG. 11



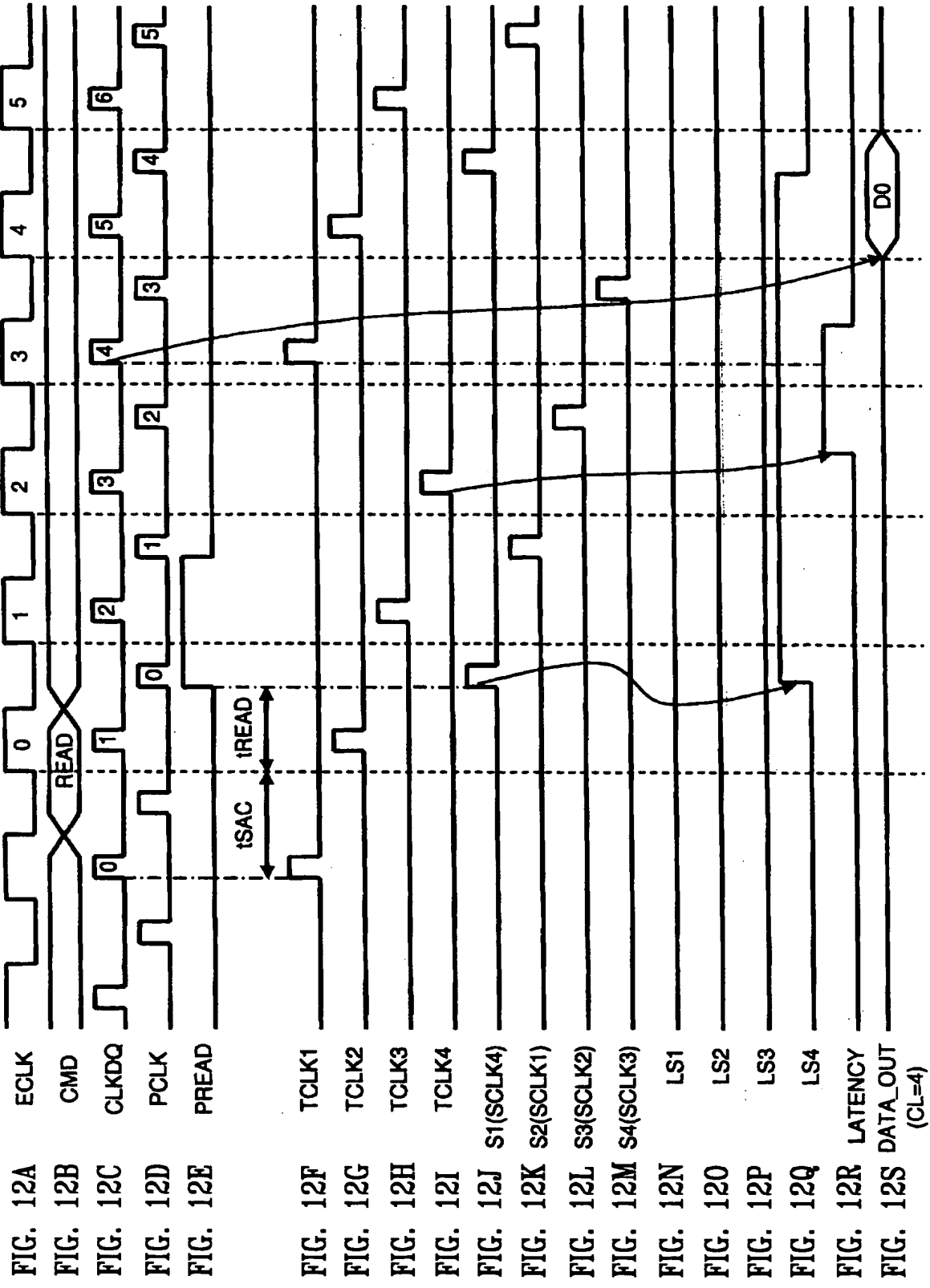


FIG. 13A

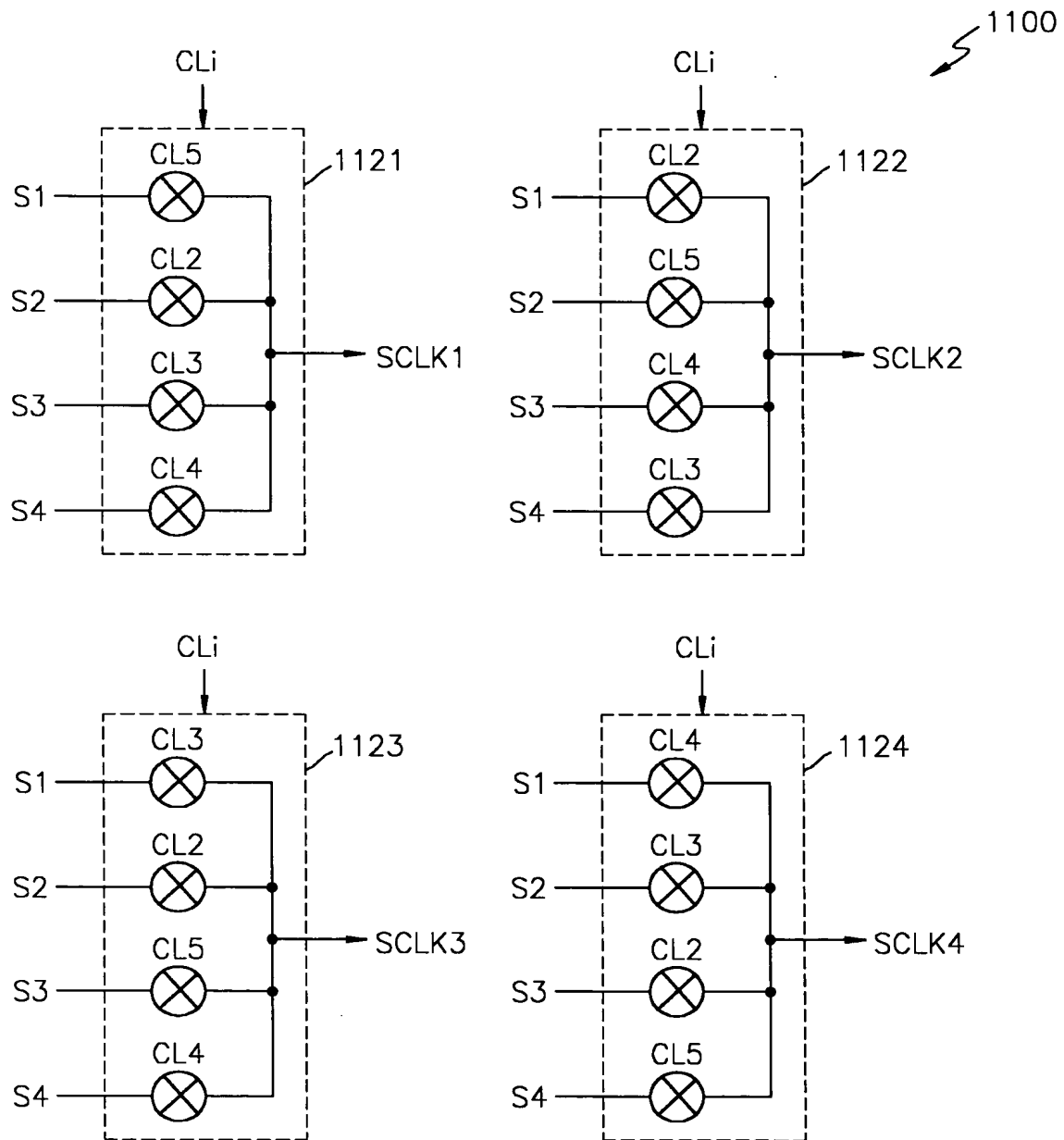


FIG. 13B

CL	SCLK1	SCLK2	SCLK3	SCLK4
2	S4	S1	S2	S3
3	S3	S4	S1	S2
4	S2	S3	S4	S1
5	S1	S2	S3	S4

FIG. 14

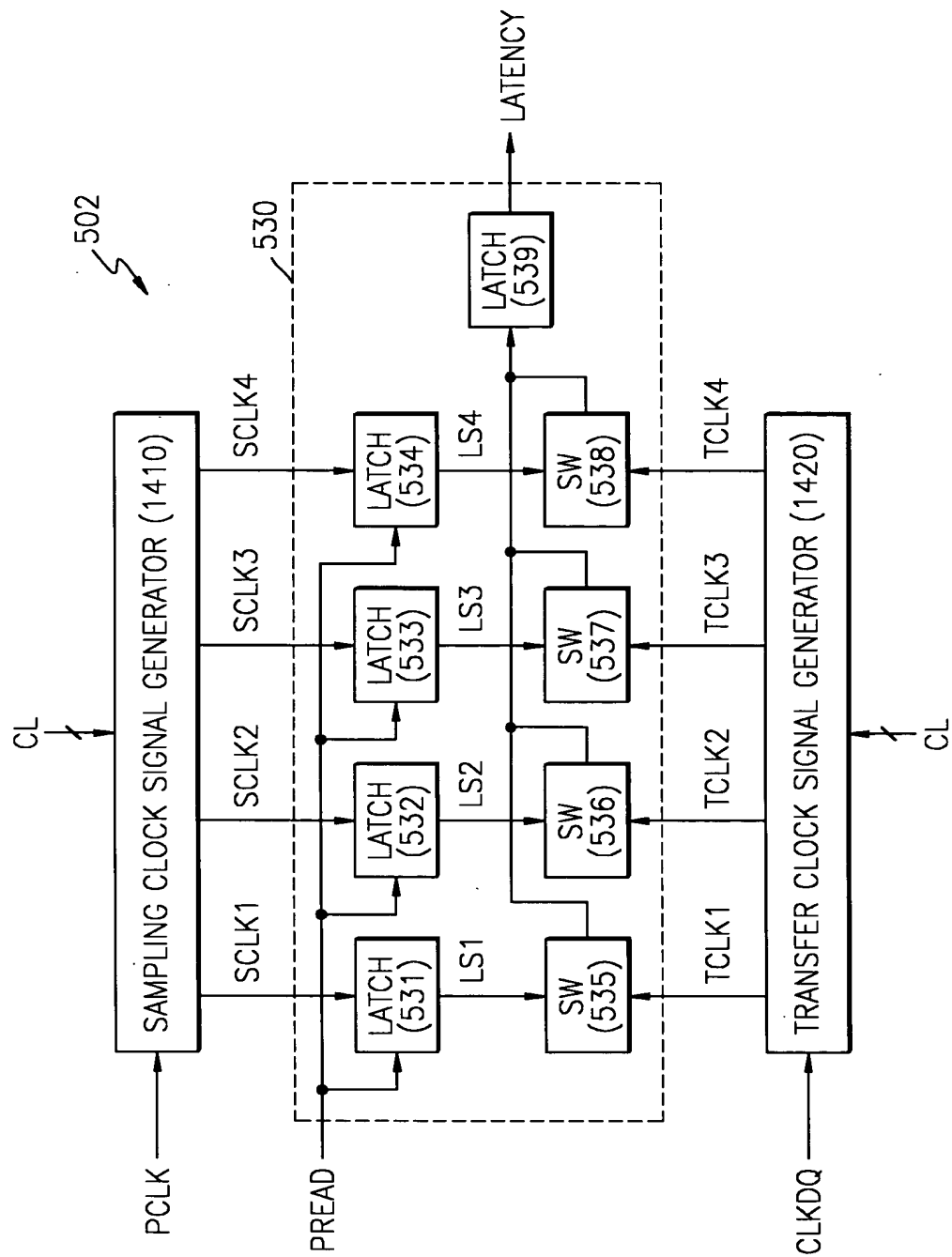


FIG. 15

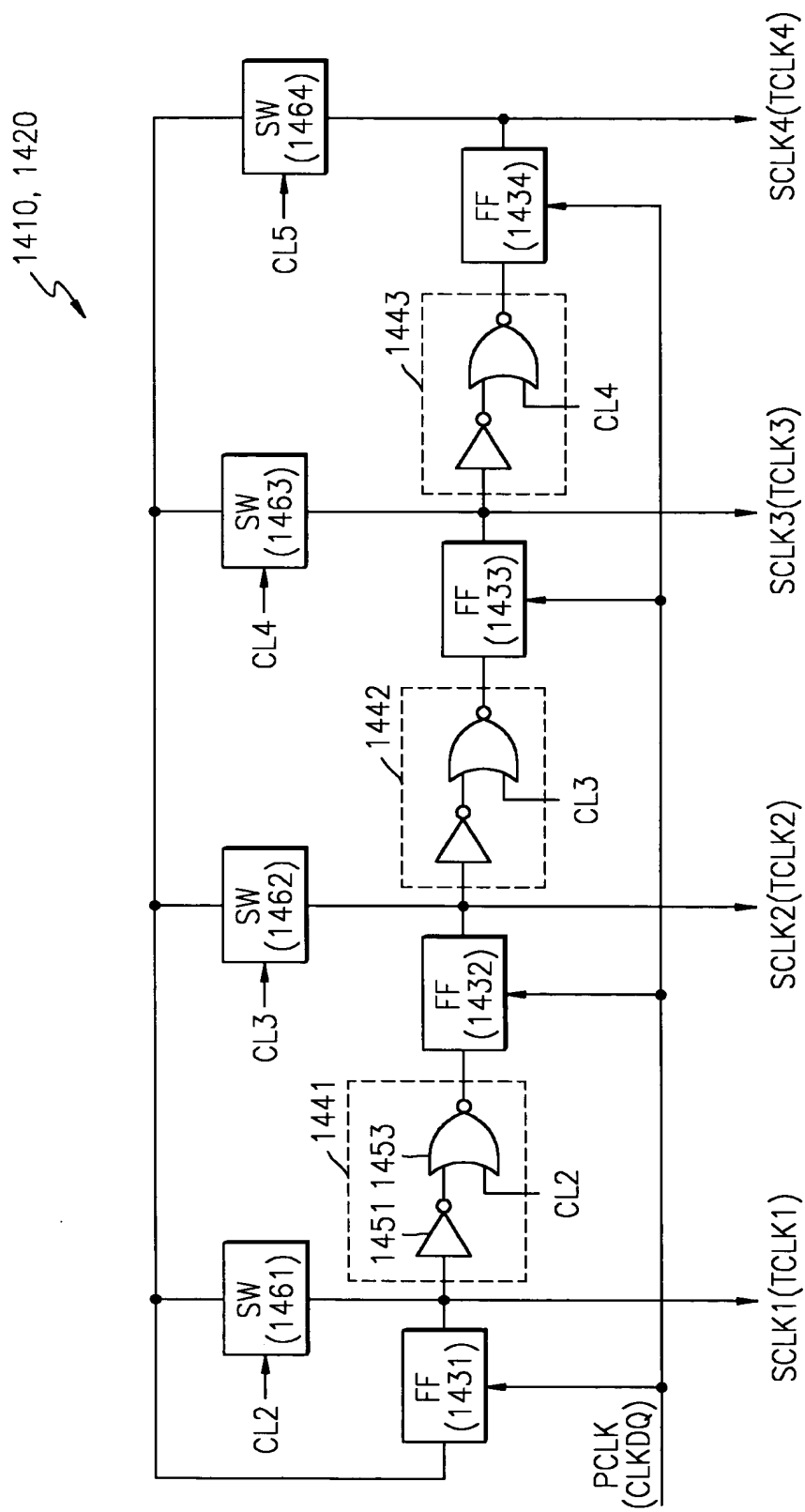


FIG. 16

CL2					CL4						
TCLK1	0		1	1	1	1	0	0	1	0	0
TCLK2	0		0	0	0	0	1	0	0	1	0
TCLK3	0		0	0	0	0	0	1	0	0	1
TCLK4	0		0	0	0	0	0	0	0	0	0

CL3					CL5						
TCLK1	0		1	0	1	0	0	0	1	0	0
TCLK2	0		0	1	0	1	0	0	0	1	0
TCLK3	0		0	0	0	0	0	1	0	0	0
TCLK4	0		0	0	0	0	0	0	1	0	0

